Appl. No. 10/694,155
Examiner: CHEN, JACK S J, Art Unit 2813
In response to the Office Action dated June 23, 2004

Date: September 9, 2004
Attorney Docket No. 10110752

REMARKS

Applicant thanks the Examiner for acknowledging Applicant's claim to foreign priority and receipt of the certified copy of the priority document in the parent to this application. Responsive to the Office Action mailed on June 23, 2004 in the above-referenced application, Applicant respectfully requests amendment of the above-identified application in the manner identified above and that the patent be granted in view of the arguments presented. No new matter has been added by this amendment.

Present Status of Application

Claims 1-10 are pending. Claims 1, 7-10 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,703,387 to Hong. Claims 1, 3-10 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,998,261 to Hofmann et al. Claims 1, 7, and 10 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,486,028 to Chang et al. Claim 2 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Hong and Hofmann et al., respectively. Claims 1-10 stand rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-16 of U.S. Patent No. 6,670,246 to Hsiao et al.

In this paper, claim 1 is amended to recite a method of forming a vertical nitride read-only memory cell comprising, *inter alia*, the step of forming a conformable insulating layer as gate dielectric on the substrate surface that constitutes sidewalls of a trench and the surface of a bit line oxide. This feature is shown in FIG. 2e of the application, wherein the gate dielectric layer 223 directly contacts the surface of substrate 200 constituting sidewalls of the trench 208. No new matter has been added.

Reconsideration of this application is respectfully requested in light of the amendments and the remarks contained below.

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Rejections under 35 U.S.C. 102(b)

Claims 1, 7-10 stand rejected under 35 U.S.C. 102(b) as being anticipated Hong. Claims 1, 3-10 stand rejected under 35 U.S.C. 102(b) as being anticipated by Hofmann et al. Claims 1, 7, and 10 stand rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. The rejections under 35 U.S.C. 102(b) are respectfully traversed for the reasons that follow.

None of Hong, Hoffman et al or Chang et al recite a method of forming a vertical nitride read-only memory cell comprising, *inter alia*, the step of forming a conformable insulating layer as gate dielectric on the substrate surface that constitutes sidewalls of a trench and the surface of a bit line oxide, as recited in claim 1.

MPEP 2131 prescribes that to anticipate a claim, a reference must teach every element of the claim. In this regard, the Federal Circuit has held:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
>
> "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim 1 recites a method for fabricating a vertical nitride read-only memory (NROM) cell, comprising the steps of providing a substrate having at least one trench; forming doping areas as bit lines in the substrate near its surface and the bottom of the trench; forming bit line oxides over each of the doping areas; forming a conformable insulating layer as gate dielectric ***on the substrate surface that constitutes sidewalls of the trench and the surface of the bit line oxide***; and forming a conductive layer as a word line over the insulating layer and filling in the trench.

In the office action, dielectric layer 50 in Hong is relied upon to teach the gate dielectric layer in claim 1. However, as described in col. 4, lines 10-12 and FIG. 9 of Hong, dielectric layer 50 is deposited onto to the exposed surface of the device. That is, the dielectric layer 50 is deposited onto the floating gate 48' formed on the sidewalls trench and does not directly contact the surface substrate 32 that constitutes the sidewalls of the trench. Accordingly, the cited reference does not teach or suggest a gate dielectric layer conformably formed on the substrate surface that constitutes sidewalls of the trench, as recited in claim 1.

The office action also relies upon second dielectric layer 12 as of Hoffman et al to teach the gate dielectric layer in claim 1. However, as described in col. 4, lines 38-56 and figs. 4-5 of Hofmann et al, second dielectric layer 12 is produced over the entire surface of the substrate shown in FIG. 4 after removal of the trench mask 6. That is, second dielectric layer 12 is formed onto the doped polysilicon spacers 11 and does not directly contact the surface of substrate 3 constituting the sidewalls of the trench. Accordingly, the cited reference does not teach or suggest a gate dielectric layer conformably formed on the substrate surface that constitutes sidewalls of the trench, as recited in claim 1.

Finally, the office action relies upon the silicon oxide layer 110 of Chang et al to teach the bit line oxides recited in claim 1, and relies upon the silicon nitride layer 112 and top silicon oxide 114 of Chang et al to teach the gate dielectric layer in claim 1, respectively. However, as described in col. 3, line 53 to col. 4, line 7 and figs. 3-5 of Chang et al., the silicon oxide layer 110 is grown over the substrate 100 and the sidewalls and bottom of trench 102. Thereafter, the silicon nitride layer 112 and top silicon oxide 114 are successively deposited over the silicon oxide layer 110. That is, the silicon nitride layer 112 and top silicon oxide 114 do not directly contact the substrate 100 surface at the sidewalls of the trench 102. Accordingly, the cited reference does not teach or suggest a gate dielectric layer conformably formed on the substrate surface that constitutes sidewalls of the trench, as recited in claim 1.

Applicant therefore submits that none of the cited references, when taken individually or in combination, teach or suggest a method for fabricating a vertical nitride read-only memory cell comprising all of the steps recited in claim 1. It is therefore Applicant's belief that claim 1 is

allowable of the cited references. Insofar as claims 2-10 depend from claim 1, it is Applicant's belief that these claims are also in condition for allowance.

Double Patenting Rejections

Attached please find a terminal disclaimer under 37 C.F.R. 1.321 to obviate the double patenting rejection over Hsiao et al. The disclaimer is made solely for the purpose of advancing the prosecution of the application and should not be construed as an admission with respect to the merits of the rejection.

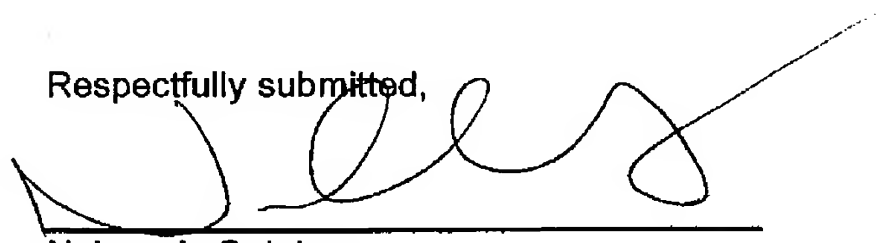
Prior Art in Earlier Application

This application is a divisional application of U.S. Patent Application Serial No. 10/318,551. The Examiner is reminded to consider the prior art cited in the parent application. MPEP 609 and 2001.06(b).

Conclusion

The Applicant believes that the application is now in condition for allowance and respectfully requests so.

Respectfully submitted,



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